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PROVISIONAL APPLICATION COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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2. TITLE OF THE INVENTION

LOW LATENCY RADIO / BASEBAND INTERFACE PROTOCOL

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4. ENCLOSED APPLICATION PARTS

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Philips Proposal for

JEDEC JC- 61

Digital Radio / Baseband Interface Standard

Author: Olaf Hirsch

Abstract:

Specification for a high speed differential Radio / Baseband interface

List of Updates

Table 1: Revision History

Issue	Date	Updated Paragraphs	Description
0.1			First Draft
0.2		1.6	Added alternative 2 to the transport layer

Table 2: List of Known Defects and Omissions

Issue	Defect Description
0.1	

Table of Contents

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Foreword

< Will be filled out at a later point in time >

- An indication of the intended user of the document
- The designation and name of the committee that prepared the standard
- Information regarding the approval of the standard by the JEDEC Board of Directors
- An indication of any other organization that has contributed to the preparation of the standard
- A statement that the standard cancels and replaces other documents in whole or in part
- A statement of significant technical changes from the previous edition of the standard
- The relationship of the standard to other standards or other documents
- A statement as to which annexes are normative and which are informative

Introduction

Features

The digital Radio / Baseband interface is a low power differential high speed serial interface loosely based on the physical layer of serial ATA. The interface has four wires two for the up-link and two for the down-link.

The interface uses an 8B/10B code to transmit the data and clock over the same interface.

In transport layer alternative 1the default configuration of the digital Radio / Baseband Interface provides a sampling data bandwidth of 800 Mbps and a control bandwidth of 320kbps at an interface latency of 100ns. Sampling data rate can be increased at the cost of a higher interface latency.

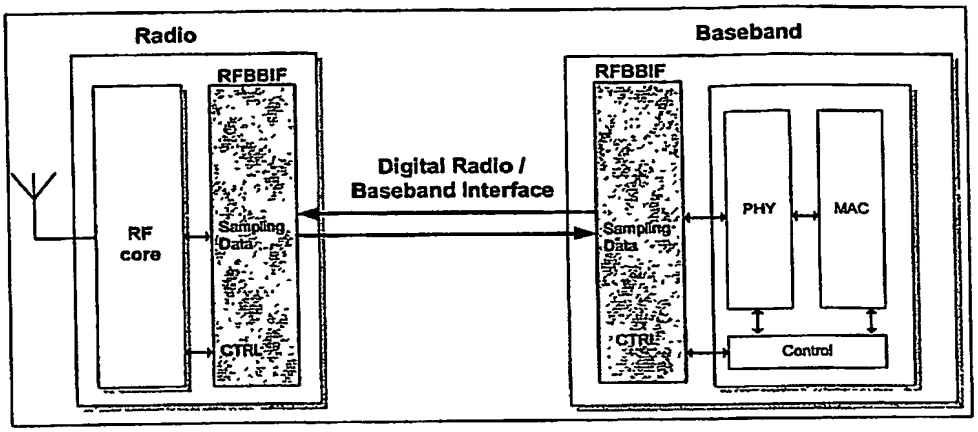
In transport layer alternative 2 the default configuration of the digital Radio / Baseband Interface provides a sampling data bandwidth of 800 Mbps the remaining bandwidth of 320Mbps is available to transmit control and other information. The interface latency in the default configuration is 18.75ns.

The interface supports most transceiver architectures. Sampling data can either be from a low IF or I/Q transceiver. The interface controls the radio either through register access or through a parallel control field.

In addition to data samples and control information the interface can transmit continuous data like RSSI values.

Place in the System

Figure 1 – Place in the System



Scope

This standard specifies a physical layer, the link layer, the transport layer and the register interface of digital Radio / Baseband interface. The functionality of the Radio or the Baseband itself and is out off the scope of this specification

Normative References

[1] IEEE 802.3z/D5.0, Media Access Control (MAC) Parameters, Physical Layer, Repeater and Management Parameters for 1000 Mb/s Operation; May 6, 1998

[2] Klaus-Peter Deyring, **"Serial ATA : High Speed Serialized AT Attachment"**, Revision 1.0, 29 August 2001, APT Technologies / Dell Computer Corporation / IBM Corporation / Intel Corporation, Maxtor Corporation / Seagate Corporation.

Terms and Definitions

For the purpose of this standard, the terms and definitions given in the following apply:

8B/10B transmission code	A DC balanced octet oriented data encoding
Baseband	Digital transceiver
Comma	A specific 8B/10B control code which is used for the purpose of frame alignment
Down-Link	Direction from the Radio to the Baseband
Frame	Data structure used to exchange data between the Radio and Baseband
Idle Frame	Frame without sampling data
Idle Period	No sampling data is transmitted
Octet	8 bits
Radio	Radio Frequency transceiver
Raw data rate	Data rate after 8B/10B encoding
Running Disparity	A binary parameter having a value of + or -, representing the imbalance between the number of ones and zeros in a sequence of 8B/10B code-groups
Sampling Data	Digital data from the ADC in the radio and for the DAC in the radio
Streaming Frame	Frame with sampling data
Up-Link	Direction from the Baseband to the Radio

Symbols and Abbreviated Terms

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
DC	Direct Current
DR	Data Ready
LSB	Least Significant Bit
RA	Register Address
RAA	Register Address Available
RD	Register Data

1 Physical Layer

1.1 Overview

The Radio / Baseband Interface has two differential pairs or four wires. One pair has the line driver on the Radio and the receiver on the baseband, the other pair has the line driver on the baseband and the receiver on the radio.

Raw data rate of the interface is 1.6Gbps in each direction.

1.2 Electrical Parameters

Table 3: Electrical parameters

Parameter	Min	Typ	Max	Units	Description
T, UI		625		ps	Operating Data period
t_{rise}	0.2	0.3	0.41	UI	20% - 80% at transmitter
t_{fall}	0.2	0.3	0.41	UI	80% - 20% at transmitter
$V_{cm,dc}$	200	250	300	mV	Common mode DC level measured at receiver. This spec only applies to direct connected designs that hold the common mode level.
$V_{cm,ac}$			100	mV	Max. sinusoidal amplitude of common mode signal measured at the receiver input.
F_{CM}		2	200	MHz	All receivers must be able to tolerate sinusoidal common-mode noise components inside this frequency range with and amplitude of $V_{cm,ac}$

Table 3: Electrical parameters

Parameter	Min	Typ	Max	Units	Description
$T_{settle,CM}$			10	ns	Maximum time for common mode transients to settle to within 10% of DC value during transitions to and from the ACTIVE bus state
$V_{diff,tx}$	400	500	600	mV_{p-p}	+/- 250 mV differential nominal. Measured at RFBBIF transmitter
$V_{diff,rx}$	325	400	600	mV_{p-p}	+/- 200mV differential nominal. Measured at the RFBBIF receiver
TX differential output impedance	85	100	115	Ohm	As seen by a differential TDR with 100ps (max) edge looking into the transmitter
RX differential input impedance	85	100	115	Ohm	As seen by a differential TDR with 100ps (max) edge looking into the receiver
TX DC clock frequency skew	-2650		+350	ppm	Includes crystal
TX differential skew			20	ps	(Nominal value architecture specific)

1.3 *Eye Diagram*

The Eye diagram in Figure 2 shows the Voltage/Timing diagram. The diagram is given for informational purposes only and is not used to verify standard compliance.

Figure 2 – Eye Diagramm

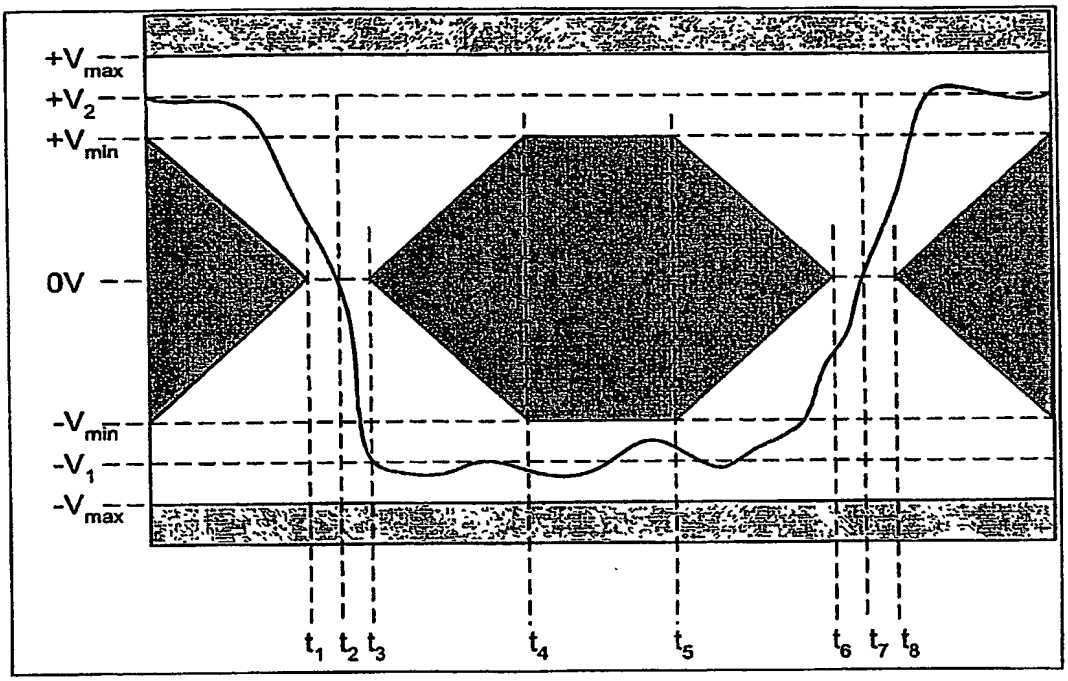


Table 4: Voltage / Timing margin definition

Name	Definition	Notes
t_{jitter}	$t_3 - t_1$	$t_3 - t_1 = t_8 - t_6$
T	$t_7 - t_2$	$t_2 - t_1 = t_3 - t_2$ $t_7 - t_6 = t_8 - t_7$
V_{diff}	$V_2 - V_1$	

1.4 Mechanical Parameters

1.4.1 Cables

To be specified at a later stage

1.4.2 Connectors

To be specified at a later stage

1.5 Link Layer

1.5.1 Data Encoding

The 8B/10B transmission code encodes an octet into a 10-bit code word. The code word is chosen as such that the code has enough zero one transitions to facilitate clock recovery in the receiver. The code is DC balanced i.e. it has the same amount of ones and zeros in a sufficiently long data stream. The running disparity of the code never exceeds one.

The transmission code supports error detection in the receiver as not all ten bit code words are valid code words.

The definition of 8B/10B transmission code in this standard is identical to that specified in ANSI X3.230-1994 (FC-PH), clause 11.

Data is sent LSB first.

1.5.2 Interface Initialization

Before the Radio / Baseband Interface is used to transmit data, it shall be initialized with a training sequence in order to phase lock the PLLs of the interface in the down-link and the up-link of the interface.

The initialization sequence shall be six repetitions (150us) of the SYNC primitive. The SYNC primitive is defined as K28.3, D21.4, D21.5, D21.5.

The 8B/10B receiver should assume either positive or negative disparity after initialization.

The initialization should start with initializing the down-link with the initialization sequence. After the down-link is initialized the up-link is initialized through the initialization sequence.

1.5.3 Interface Power Modes

The interface has four states: OFF, SLEEP, ACTIVE and CLOCK.

During ACTIVE state control communication and data streaming in both directions is possible.

The SLEEP state is entered by programming register rfbbif_state to the SLEEP state. After the command is issued the baseband and radio can switch-off the interface. The state of the baseband and the radio itself is implementation dependent.

In order to transition out-off SLEEP state the baseband switches on the common mode signal for the up-link. The Radio switches on the common mode signal for the down-link and starts the initialization sequence. Once the initialization sequence is completed the interface enters ACTIVE state.

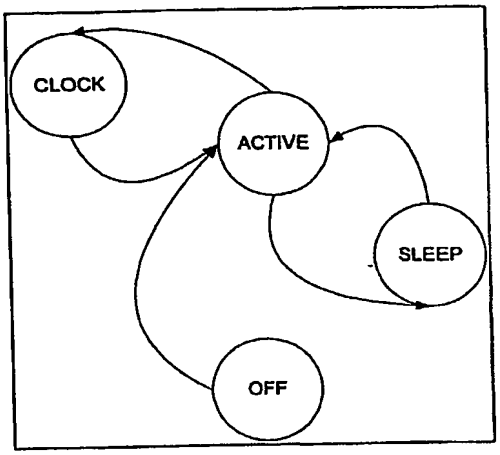
CLOCK state is a special power down state in which only the down-link of the interface stays active to provide the timing reference for the baseband. The up-link is powered off. The CLOCK state is entered by programming register rfbbif_state to CLOCK state in the radio. After the command is issued the PHY and radio can power down the up-link. Once powered down the interface enters the CLOCK state.

In order to leave the CLOCK state to ACTIVE state the PHY applies the common mode signal to the up-link. 10 ns later the baseband sends one SYNC primitive to the RF-FE. After the SYNC primitive has been sent the Radio / Baseband Interface enters the ACTIVE state.

The interface is in OFF state while the system is not powered up. The OFF state is automatically exited after power-up of the system. In order to exit the OFF state after power-up the radio switches on its reference oscillator. The reference clock is optionally supplied to the baseband. The radio executes the initialization sequence. After executing the initialization sequence the interface transitions to the ACTIVE state.

The interface can enter the OFF state from all states by switching off the power of the system. Figure 3 shows the state diagram for the Radio / Baseband Interface. The transition into the OFF state are not shown.

Figure 3 – Radio / Baseband State Diagram



1.5.4 Radio / Baseband Synchronization

The oscillator in the Radio shall be the timing master in ACTIVE and CLOCK state. All clocks in the baseband relevant to the synchronization of the system shall be phase locked to this oscillator. This shall be done by keeping the down-link of the interface active with an random 8B/10B code sequence.

In SLEEP state the phase lock can be broken in order to save power. The baseband can use a different clock or oscillator during SLEEP state. Before entering ACTIVE state the baseband shall phase lock its clock with the radio again.

The up-link shall be phase locked to the down-link of the Radio / Baseband Interface

1.6 Transport Layer

1.6.1 Radio / Baseband Frame (Alternative 1)

1.6.1.1 Protocol

Figure 4: Radio / Baseband Frame Protocol

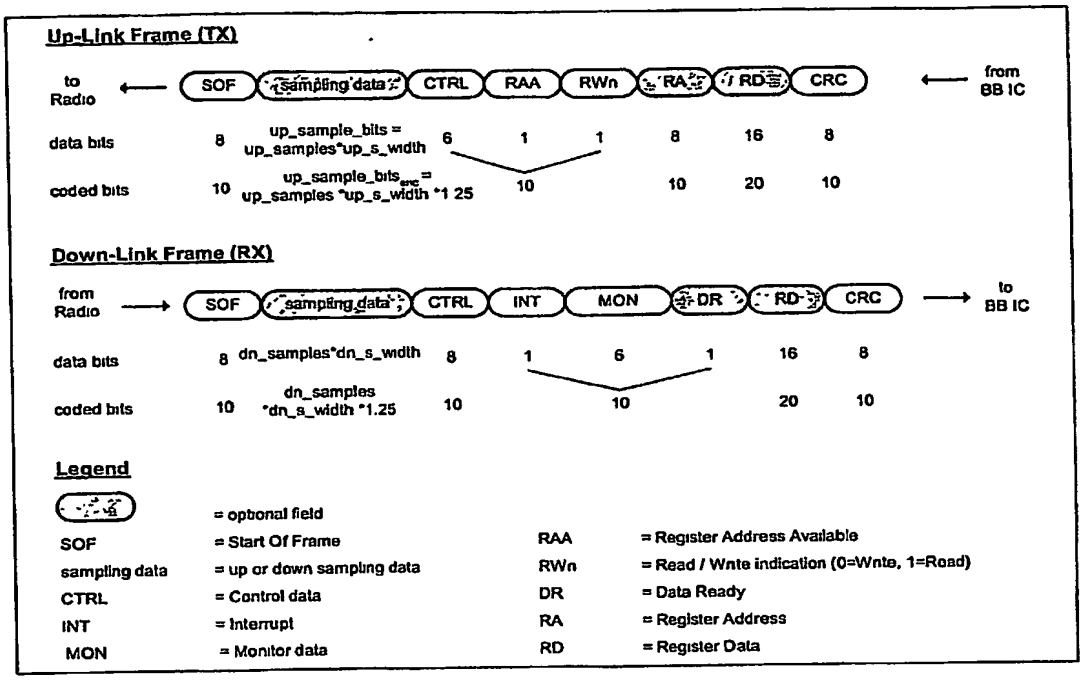


Figure 5 shows the Radio / Baseband frame protocol. Two frame formats have been defined; one for the up-link, and one for the down-link. Each frame starts with a SOF symbol followed by the sampling data field , one or more multi-purpose control fields, and some fields that together provide access to the registers inside the Radio. Each frames ends with a CRC field.

A detailed description of the fields is given in the chapters below.

The frame length is determined by the latency requirements for time-critical control signals that have to cross the Radio / Baseband Interface (e.g. AGC control). The average allowable frame length is given by:

$$frame\_length_{enc} = f_{clk} \times t\ latency(max)$$

For an interface latency of 100ns and a frequency of 1.6GHz the average frame length is given by:

$$frame\_length_{enc} = 1.6x10^{9} \times 100x10^{-9} = 160 \text{ bit.}$$

The frame length before 8B/10B encoding is given by:

$$frame\_length = 160 \times 8/10 = 128bit = 16 \text{ bytes}$$

Due to optional fields, the actual frame length can vary. The different configuration options for the RF-BB frames are shown in Table 5 and Table 6 for 10 sampling data samples.

Table 5 – Radio / Baseband Up-Link Frame

SOF	RAA	RWn	Sample Field	RA field	RD field	Frame length coded bits	Frame length data bits
			Streaming Frame				
SOF1	0	X	yes	no	no	3 x 8 = 104	13 x 10 = 130
SOF1	1	0	yes	yes	yes	16 x 8 = 128	16 x 10 = 160
SOF1	1	1	yes	yes	no	14 x 8 = 112	14 x 10 = 140
			Idle Frame				
SOF2	0	X	no	no	no	3 x 8 = 24	3 x 10 = 30
SOF2	1	0	no	yes	yes	6 x 8 = 48	6 x 10 = 60
SOF2	1	1	no	yes	no	4 x 8 = 32	4 x 10 = 40

Table 6: Radio / Baseband Down-Link Frame

SOF	DR	Sample Field	RD Field	Frame Length Coded Bits	Frame Length Data Bits
		Streaming Frame			
SOF1	0	yes	no	14 x 8 = 112	14 x 10 = 140
SOF1	1	yes	yes	16 x 8 = 128	16 x 10 = 160
		Idle Frame			
SOF2	0	no	no	4 x 8 = 32	4 x 10 = 40
SOF2	1	no	yes	6 x 8 = 48	6 x 10 = 60

The frame length shall be such that the average over two frames equals frame_length data bytes or less. If no sampling data is transmitted the frame length is reduced considerably. This has the benefit that the latency for Idle Frames can be up to 80% shorter than the latency for Streaming Frames => 20ns. This is very important in time-critical loops, like e.g. the AGC.

If no frames are to be send on the up-link or down-link the interface inserts random 8B/10B symbols between frames.

1.6.1.2 Start of Frame

The SOF field defines the start of frame preamble. Two different preambles are used to differentiate between streaming frames (SOF1) and idle frames (SOF2).

SOF1 is chosen to be the 8B/10B control character K28.1 and SOF2 is control character K28.7. Both characters are comma characters to facilitate frame synchronization.

1.6.1.3 Sampling Data Fields

The sampling data field is only available in streaming frames. The sampling data field contains the up- or down-link sampled data from the ADCs and DACs in the radio.

The sampling data field shall only be used together with the SOF2 symbol.

dn_samples and up_samples defines the number of sampling data samples in the down- and up-link, respectively. dn_s_width and up_s_width define the number of bits in each sample for the down- and up-link, respectively. dn_sample_bits and up_sample_bits define the number of bits in the sampling data field for the down- and the up-link, respectively. $dn\_sample\_bits_{enc}$ and $up\_sample\_bits_{enc}$ define the number of 8B/10B encoded bits in the sampling data field for the down- and the up-link, respectively.

The recommended number of sampling data samples is set to eight and has been chosen such that it corresponds with the 40Msamples/sec sample rate of the I/Q samples or 80Msamples/sec for IF samples to/from a 802.11g baseband. This reduces the amount of buffering that is required for the data samples, and minimizes the interface latency for the data samples.

1.6.1.4 Control Fields

The CTRL field is used for time-critical control signals, like AGC, but it can also be used to signal events that are not necessarily time-critical but can occur simultaneously to other signals. The up-link CTRL field is 6 bit wide and the down-link CTRL field is 8 bits wide.

The MON field in the down-link can be used to monitor values in the radio like RSSI.

The usage of the CTRL and MON fields depends on the radio manufacturer.

1.6.1.5 Register Data

A R/W register access to the radio shall be initiated by an up-link frame. The RAA field (Register Address Available) shall be set to one to indicate that the baseband accesses one of the registers in the

radio. The current frame shall include the address of the register that needs to be accessed. For a read access the RWn field shall be set to one, for a write access the RWn field shall be set to zero.

In case of a write transaction the up-link frame shall include the register data that needs to be written to a radio register in the RD field. In case of a read transaction one of the next down-link frames returns the register read data to the baseband in the RD field. The register value shall be returned on the down-link no later than 50 ns or one frame in case of streaming data frames in the down-link.

The DR field (Data Ready) shall set to one, if the RD field contains a valid register value. In all other cases the DR field shall be set to zero.

No new register shall be read until the previous read has been received in the down-link by the baseband. The RA and RD fields in the up-link and down-link frames are optional and only required when a register in the radio needs to be read or written. The presence of the RA and RD fields is determined by the values of the RAA field and the R/W field.

1.6.1.6 Cyclic Redundancy Check

The 8-bit CRC field is the last field in the frame and contains the result of the CRC calculation. The CRC value in the up-link is calculated over all data in the data in the frame after the SOF field. In the down-link the CRC is calculated over all data in the frame after the SOF field. On transmission the CRC shall be calculated before 8B/10B encoding, on reception the CRC shall be calculated after 8B/10B decoding.

The CRC polynomial is g(x) = x8 + x2 + x + 1. The CRC is calculated starting from an all zero state.

1.6.2 Radio / Baseband Frame (Alternative 2)

1.6.2.1 Protocol

Figure 5: Radio / Baseband Frame Protocol

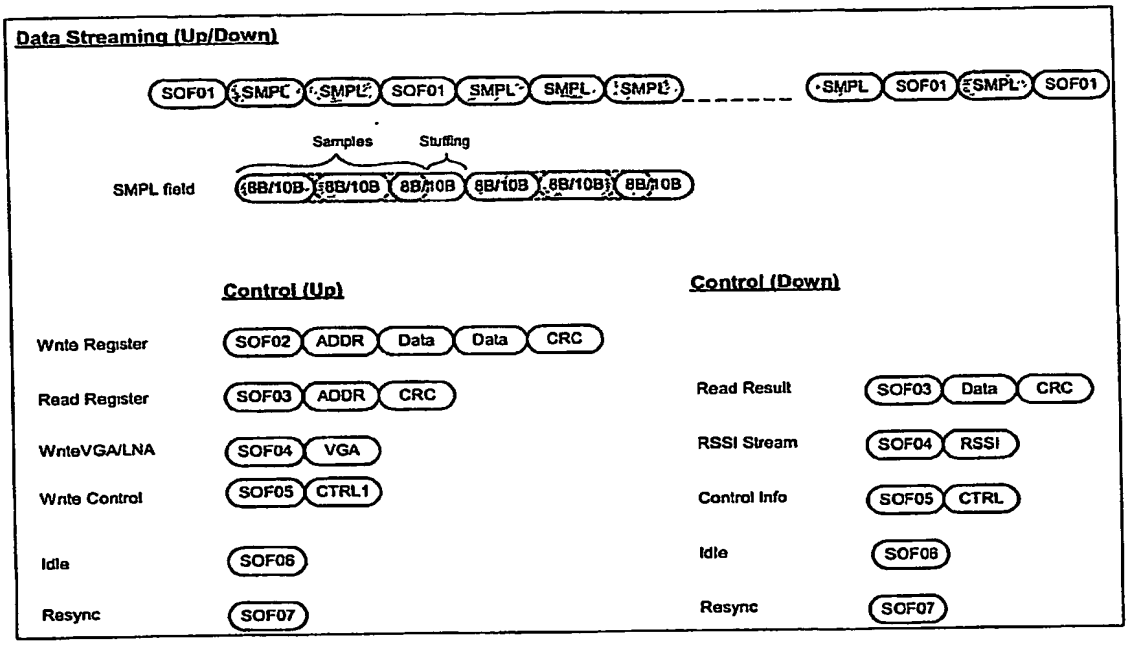


Figure 5 shows the Radio / Baseband frame protocol. Several frame and streaming formats have been defined.

The transmission of a particular type of data stream or frame type is initiated by a 8B/10B control word. Table 7 lists the defined control words.

Table 7: SOF Identifier

SOF Identifier	8B/10B control word	Description
SOF01	K28.1	Streaming data samples, 8B/10B comma character
SOF02	K28.0	Write register
SOF03	K28.2	Read Register / Read Result
SOF04	K28.3	Write VGA/LNA / RSSI Stream

Table 7: SOF Identifier

SOF Identifier	8B/10B control word	Description
SOF05	K28.4	Write Control / Control Info
SOF06	K28.6	Idle Period
SOF07	K28.7	Resync, comma character
SOF08 - 12	K28.5, K23.7, K27.7, K29.7, K30.7	Reserved

1.6.2.2 Data Streaming

Data streaming is initiated with the SOF01 control word. Sampling data follows the initial control word. SOF01s are also inserted to adapt the data rates between the sampling data and the interface rate.

During data streaming the other control frames are just inserted instead of the SOF01 rate adaptation symbols. At the end of an inserted control frame the transmission of data samples resumes without the requirement to send an additional SOF01 symbol.

1.6.2.2.1 Data Sample Field

The number of data samples and the bits per sample in the SMPL field is programmable through register access. If the number of bits in the SMPL is not a multiple of 8 the SMPL field is padded with zeros.

This leaves the sample field to be extremely flexible as it could contain a single sample in case of a low IF radio, one I/Q sample pair or multiple samples.

1.6.2.3 Idle Frame

Idle frames are transmitted if no data samples have to be transmitted. The frame starts with a unique SOF06 symbol followed by random data. Approx. every 1000 data symbols a SOF07 symbol is inserted to facilitate resynchronization of the interface in case of a transmission error. Control frames are inserted into the idle frame stream in the same way as it is done for the data sample stream.

1.6.2.4 Write Register

The write register frame can be inserted into a data sample stream or an idle period at any time. The frame starts with the unique SOF02 control word followed by eight address bits and 16 data bits. In order to provide additional error detection capability the frame ends with an 8 bit CRC.

1.6.2.5 Read Register

The read register frame can be inserted into a data sample stream or an idle period at any time. The frame starts with the unique SOF03 control word followed by eight address bits. In order to provide additional error detection capability the frame ends with and 8 bit CRC. On arrival of a read register frame in the radio the radio reads the internal register. The interface places the register value in the read result frame on the down link and inserts the frame at any time into the data sample stream or into an idle period.

1.6.2.6 Write VGA/LNA

The write VGA/LNA frame can be inserted into a data sample stream or an idle period at any time. The frame starts with the unique SOF04 control word followed by eight bits for the VGA/LNA settings.

1.6.2.7 Write Control

The write control frame can be inserted into a data sample stream or an idle period at any time. The frame starts with a unique SOF05 control word followed by eight control bits. The control bits can be used to enable the PA, switch the antenna or switch between Rx and Tx.

1.6.2.8 RSSI Stream

The RSSI Stream frame can be inserted into a data sample stream or an idle period stream in the down link at any time. The frame stars with a unique SOF04 control word followed by an eight bit RSSI value. The rate of the RSSI Stream frame is programmable. The user has to make sure that the combined data rate of the data sample stream and the RSSI stream frame does not exceed the bandwidth of the interface.

1.6.2.9 Control Info

The control info frame can be inserted into a data sample stream or and idle period stream in the down link at any time. The frame starts with a unique SOF05 word followed by eight control bits. The control bits can be used to indicate interrupts or other events generated by the radio. A control frame is send every time a control signal changes.

1.6.2.10 Cyclic Redundancy Check

The 8-bit CRC field is the last field in the register access frames and contains the result of the CRC calculation. The CRC value in the up-link is calculated over all data in the data in the frame after the SOF field. In the down-link the CRC is calculated over all data in the frame after the SOF field. On transmission the CRC shall be calculated before 8B/10B encoding, on reception the CRC shall be calculated after 8B/10B decoding.

The CRC polynomial is $g(x) = x8 + x2 + x + 1$. The CRC is calculated starting from an all zero state.

1.6.2.11 Transmission Error Handling

After detection of a CRC error or 8B/10B decoding error the in the down link, the baseband sends a register access frame requesting the radio to transmit a Resync frame (SOF07).

If a CRC error or 8B/10B deciding error is detected in the up link, the radio sends a control info frame to the baseband requesting a Resync frame (SOF07).

Further error recovery after a CRC error or 8B/10B decoding error is implementation dependent.

2 Radio Interface Registers

2.1 General

The Radio / Baseband interface standard requires a number of registers in the radio to configure and control the interface. Registers in the radio defining the functionality of the radio itself are out of the scope of this specification.

2.2 Register Overview

Table 8: Radio / Baseband Register Overview

Register Name	Address	Access	Description
rfbbif_reset	0x0	W	Writing to the register will cause the interface and the radio to reset
rfbbif_state		R/W	Defines the interface states: ACTIVE, SLEEP, CLOCK
rfbbif_int_flag		R/W	Interrupt flag register
rfbbif_in_en		R/W	Interrupt enable register
rfbbif_ctrl		R/W	Interface control register
rfbbif_smpl		R/W	Interface data sample format register
rfbbif_man		R	Manufacturer code
rfbbif_ver		R	Radio version number
rfbbif_jc61		R	JEDEC JC-61 Radio / Baseband interface version compliance

2.3 Registers

Table 9: RFBBIF_RESET – Radio / Baseband Reset Register

Legend: * reset value; ~* reset value not defined

Bit	Symbol	Access	Value	Description
15:0	RESET	W		Write to register resets the interface

Table 10: RFBBIF_STATE – Radio / Baseband State Register

Legend: * reset value; ~* reset value not defined

Bit	Symbol	Access	Value	Description
15:2	Reserved			Read and write as zero
1:0	STATE	R/W		Interface state definition. When written the interface transitions into the new state. Transitions from SLEEP and CLOCK are not possible be writing to this register (see chapter 1.5.3)

Table 11: RFBBIF_INT_FLAG – Radio / Baseband Interrupt Flag Register

Legend: * reset value; ~* reset value not defined

Bit	Symbol	Access	Value	Description
15:2	Reserved			Read and write as zero
1	8B_10B_ERROR	R/W		8B/10B decoding error (reset if read)
			0x0*	No error detected
			0x1	Error detected
0	CRC_ERROR	R/W		CRC error (reset if read)
			0x0*	No error detected
			0x1	Error detected

Table 12: RFBBIF_INT_EN – Radio / Baseband Interrupt Enable Register

Legend: * reset value; ~* reset value not defined

Bit	Symbol	Access	Value	Description
15:2	Reserved			Read and write as zero
1	8B_10B_ERROR	R/W		8B/10B decoding error interrupt enable
			0x0*	Interrupt disabled

Table 12: RFBBIF_INT_EN – Radio / Baseband Interrupt Enable Register

Legend: * reset value; ~* reset value not defined

Bit	Symbol	Access	Value	Description
			0x1	Interrupt enabled
0	CRC_ERROR	R/W		CRC error interrupt enable
			0x0*	Interrupt disabled
			0x1	Interrupt enabled

Table 13: RFBBIF_CTRL – Radio / Baseband Interface Control Register

Legend: * reset value; ~* reset value not defined

Bit	Symbol	Access	Value	Description
15:4	Reserved			Read and write as zero
3	I_Q	R/W[1]		Multiplexed I/Q values (I first) or low IF samples
			0x0*	Low IF
			0x1	I/Q
2	LOOP	R/W		Loop back mode for streaming data
			0x0*	Disabled
			0x1	Enabled
1	xMODE_UP	R/W		Type of frames transmitted in the up-link
			0x0*	Idle Frames
			0x1	Streaming frames
0	MODE_DOWN	R/W		Type of frames transmitted in the down-link
			0x0*	Idle Frames
			0x1	Streaming Frames

[1] Read only for Radios with either I/Q or low IF output

Table 14: RFBBIF_SMPL – Radio / Baseband Interface Data Sample Format Register

Legend: * reset value; ~* reset value not defined

Bit	Symbol	Access	Value	Description
15:8	SAMPLES	R/W[1]	0x8*	Data samples per Frame in alternative 1 or data samples per SMPL field
7:0	WIDTH	R/W[1]	0xA*	Bits per data sample

[1] Read only for Radios with fixed frame format

Table 15: RFBBIF_MAN – Radio / Baseband Interface Manufacturer Identification Register

Legend: * reset value; ~* reset value not defined

Bit	Symbol	Access	Value	Description
15:0	ID	R		Manufacturer ID assigned by JEDEC JC-61

Table 16: RFBBIF_VER – Radio / Baseband Interface Manufacturer Version Register

Legend: * reset value; ~* reset value not defined

Bit	Symbol	Access	Value	Description
15:8	MAJOR	R		Major Version Number of the Radio
7:0	MINOR	R		Minor Version Number of the Radio

Table 17: RFBBIF_JC61 – Radio / Baseband Interface JEDEC JC-61 Version Register

Legend: * reset value; ~* reset value not defined

Bit	Symbol	Access	Value	Description
15:8	MAJOR	R		Major Version Number of JDEC JC-61 Supported by the Interface
7:0	MINOR	R		Major Version Number of JDEC JC-61 Supported by the Interface

3 Test Methods

To be specified later

RETURN COPY OF THE ID ABSTRACT TO:
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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION

DISCLOSURE OF INVENTION

THIS DESCRIPTION SHOULD BE SUPPLEMENTED BY ATTACHING COPIES OF RELEVANT DOCUMENTS, SUCH AS PUBLISHED ARTICLES OR PATENTS, PRODUCT BROCHURES, ENGINEERING NOTEBOOK PAGES AND DRAWINGS.

DESCRIPTIVE TITLE OF THE INVENTION:

Low Latency Radio / Baseband Interface Protocol

DOCKETED✓

INVENTOR #1: Olaf Hirsch (Name (Print)) | System Architect (Job Title) | Philips Semiconductors, San Jose, Ca (Division / Location)

Olaf.Hirsch@philips.com (E-Mail address) | Peter Meyer (Manager's Name)

563 S Taaffe St. Sunnyvale, CA 94086, (Home Address) | Germany (Country of Citizenship)

Described in Alternative 2 of attachment.

[redacted]

1. PRIMARY CONTACT
Who should CIP contact for further technical information about the invention and information about its planned use or public disclosure?

Inventor Name: Olaf Hirsch

2. PRESENT STAGE OF THE INVENTION

x Idea ☐ Research ☐ Development ☐ Manufacture

3. GOVERNMENT CONTRACT INVENTION

Was the invention made under a government contract? ☐ Yes x No

4. **PLEASE PROVIDE A TWO OR THREE SENTENCE SUMMARY OF YOUR INVENTION and include and underline KEY WORDS which might be useful in searching for relevant patents or publications:**

The invention describes a low latency protocol for a radio baseband interface. The invention is based on codes like 8b/10b which have defined control characters and data characters. The control characters mark the beginning of a frame or are being used for rate adaptation purposes The data characters are used to transmit information data between the radio and the baseband. This allows the frame structure of the protocol to be very flexible. The flexible frame structure is used to define a low latency protocol

5. PRESENT STATE OF THE ART
Briefly describe the closest already-known technology that relates to the invention. This would include, for example, already existing products, methods or compositions which are known to you personally or through descriptions in publications.

Present radio baseband protocols either implement a rigid frame structure or require header identifier to identify the following data type. Since these protocols don't use 8b/10b codes they cannot make use of the properties of 8b/10b codes to define their header identifiers. This means that header information and data information don't use different codes. This requires a protocol to be less flexible.
8B/10B codes are also used in IEEE802.3z and serial ATA but not as defined in the invention

(ADD LINES AS NECESSARY, IF COMPLETING ON COMPUTER, OR ATTACH ADDITIONAL PAGES)

6. ADVANCEMENT IN STATE OF THE ART
Briefly describe the unique advancement achieved by the invention. This may be done, for example, by describing a problem with the prior art that is solved or specific objects that are achieved by the invention.
The invention describes a low latency protocol for a radio baseband interface which uses the features of 8b/10 code words

(ADD LINES AS NECESSARY, IF COMPLETING ON COMPUTER, OR ATTACH ADDITIONAL PAGES)

7. WHAT IS THE BEST WAY YOU KNOW OF TO IMPLEMENT THE INVENTION?

[redacted]

Briefly describe the invention and how it achieves the advancement described in paragraph 7.

Please see attached document

(ADD LINES AS NECESSARY, IF COMPLETING ON COMPUTER, OR ATTACH ADDITIONAL PAGES)

*******PLEASE NOTE: IF WE DECIDE TO FILE AN APPLICATION ON THIS INVENTION, THE ATTORNEY WRITING THE APPLICATION WILL NEED THIS INFORMATION FROM YOU IN AS MUCH DETAIL AS POSSIBLE IN ORDER TO COMPLETE THE APPLICATION.

8. DISCLOSURE OUTSIDE OF PHILIPS

If the invention has been or will be disclosed publicly or to anyone other than a Philips' employee, describe to whom (person / company), date and where.
The invention will be disclosed outside of Philips on Oct 2, 2002

9. PUBLICATION

Has a description of the invention been published or submitted for publication? ☐ Yes x No
If "yes", please list each occurrence:

Date	Publication/Submission

10. PLEASE INDICATE THE PRODUCT OR SERVICE IN WHICH YOUR INVENTION MOST LIKELY WILL BE USED:

In WLAN products which use a digital radio/baseband interface

INVENTOR #1:

Signature Date